Design Simulation and characterization of op amp based 3 Bit R-2R ladder DACs

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Abstract **- This paper presents a study on a digitally calibrated DAC, based on a strictly R-2R topology with operational amplifier which is able to derive high resolution - high performance DACs, in terms of INL and DNL. It has been proven by simulations that the performance of the conventional R-2R DAC can be optimized, regardless of resistors tolerance and the DAC resolution.**

Keywords--- **Digital to analog conversion, resolution, linearity, INL, DNL, glitch.**

I. INTRODUCTION

Digital to Analog Conversion performance is mainly characterized by its resolution, linearity and speed. Additional implementation characteristics include area and power dissipation. This paper presents a DAC architecture based on the conventional R-2R ladder topology that is able to derive a high-resolution, high-linearity and high-speed DAC. Probably the most popular digital-to-analog converter application is the digital audio compact disc player. Here digital information stored on the CD is converted into music via high precision DACs.

Here an *N-bit* digital word is mapped into a single analog voltage. Typically, the output of the DAC is a voltage that is some fraction of a reference voltage or current, such that

$$VOUT = FVREF$$

Where V_{out} *is* the analog voltage output, V_{ref} is the reference voltage, and *F* is the fraction defined by the input word, *D*, that is *N* bits wide. The number of input combinations represented by the input word *D* is related to the number of bits in the word by Number of input combinations = 2^N A 3-bit DAC has a total of 2^3 or 8 total input values.

A converter with 3-bit resolution is able to map a change in the analog output which is equal to 1 part in 16. The maximum analog output voltage for any DAC must be limited by the value of some reference voltage *VREF*.

If the input is an *N-bit* word, then the value of the fraction, *F*,
can be determined by,

$$F = D/2^N$$

The *least significant bit (LSB)* refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. The LSB will always be denoted as *Do.* One LSB can be defined as

$$1\ LSB = V_{REF}/2^n$$

The *most significant bit (MSB)* refers to the leftmost bit of the digital word, *D.* Generalizing to the N-bit DAC, the MSB would be denoted as *DN-1*•

Here the maximum analog output voltage that can be generated is known as *full-scale voltage, VFS '* and can be generalized to any *N-bit* DAC as

$$V_{FS} = \left(\frac{2^n - 1}{2^n}\right) V_{ref}$$

Full scale voltage is the highest analog output voltages.

1. Differential Nonlinearity

Non ideal components cause the analog increments to differ from their ideal values. The difference between the ideal and non ideal values is known as *differential Non linearity,* or *DNL* and is defined as,

DNLn = Actual increment height of transition *n* - Ideal increment height

2. Integral Nonlinearity

Another important static characteristic of DACs is called *integral nonlinearity (INL).*

INL is defined as the difference between the data converter output values and a reference straight line drawn through the first and last output values, INL defines the linearity of the overall transfer curve and can be described as

INL = Output value for input code *n* - Output value of the reference line at that point

3. Mismatch Error related to DAC

The accuracy of the resistor string is obviously related to matching between the resistors, which ultimately determines the INL and DNL for the entire DAC. Suppose that the *i-th* resistor, *Rj* , has a mismatch error associated with it so that

$$Ri = R + \triangle Ri$$

Where *R* is the ideal value of the resistor and AR; is the mismatch error. Also suppose that the mismatches were symmetrical about the string so that the sum of all the mismatch terms were zero, or

$$= \sum_{i=1}^{2n} \Delta \, Ri = 0 \qquad \text{For } 1 = 0, 1, 2, \ldots\ldots, 2^n - 1$$

However, including the mismatch, the actual value of the *i-th* voltage will be the sum of all the resistances up to and including resistor *I*, divided by the sum of all the resistances in the string, this can be represented by,

$$Vi = V_{ref} \frac{\sum_{k=1}^{i} Rk}{\sum_{k=1}^{k} Rk} = \frac{\sum_{k=1}^{i} R + \Delta R}{2^n R}$$

or finally, the value of the voltage at the *i-th* tap is

$$Vi = Vi,ideal + \frac{Vref}{2^N} * \sum_{k=1}^{i} \frac{\Delta RK}{R}$$

Above Equation is not of much importance by itself, but it can be used to help determine the nonlinearity errors.

II. DAC ARCHITECTURE

1. Introduction

The value of CMOS resistor can be defined from below equation with the equation. And the resistance of a MOSFET operated in the linear mode is given by

$$R = V_{DS}/I_D$$

Where the V_{DS} = drain-source voltage

I_D = drain current

The drain-source voltage and the drain current are related by

$$I_{D=u.Co\,x} * \frac{W}{L} * (Vgs - Vt) * V_{DS}$$

For Vds <<< (Vgs -Vt)

Where value of W and L are variable, but there ratio will maintain the proper I_D value.

2. Operation of Designed DAC

An example of a 3 –bit R-2R MOS converter is shown in figure A. in this figure R-2R cell shown with a possible combination with the bit current switch. All transistors in this system are equal.

Depending upon the input current 2I, transistor M1 and M2 divide the input current 2I.

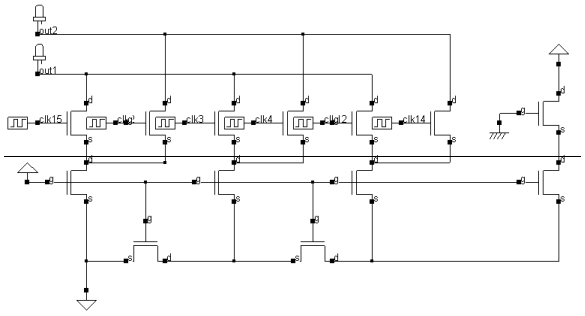

Fig A : 3 Bit R-2R MOS Converter

Transistors M1 and M2 can operate in saturated mode or in a triode mode. In saturated mode transistors M1 and M2 divide the input currents 2I in to two equal currents I. in this case transistor M3 acts as a cascade transistor and supplies the output currents to the load.

At the moments transistors m1 and M2 are in triode region, then these transistors can be seen as a resistor with value R. in this case transistor M3 performs an equal resistor of value R. in this way R-2R network is implemented and with careful termination an accurate binary weighted current division is obtained. However it is possible to include the switches in to the network by adding transistor M4.at the moment data is high, then transistor M3 is used in the network as described before and the output current I out=I_1 is supplied to the load .at the moment data bar is high, then transistor M4 is used in the network as described before and the output current I out Bar =I_2 is supplied to the load

By cascading method the basic elements of 3-bit converter can be designed as shown in fig **A**. the transistor system can be scaled depending upon the current value flowing through the individual stages. In this system trail current 8I is divided by 4I, 2I, I and I .the extra current I is obtained in the last stage

Is supplied to the bias voltage and it is not required for the digital to analog converter. With large size of the division transistor it is possible to obtain 10 bit resolution with +/- 0.5% linearity.

An accurate switching of the current is required to obtain a small glitch when the digital to analog converter is switched around the MSB values .in the offset then transistor M4 is used in the network as described before and the output current I out Bar =I_2 is supplied to the load

Biggest problem in R-2R DACs is mismatching of resisters values. This creates error in resolution. Resolution can be achieved by using operation amplifier or Low pass filter as a next stage. Proper switching is also very important.

III. OPERATIONAL AMPLIFIER ARCHITECTURE

The complete schematic of the ladder including the biasing for the op-amp is as per given below.

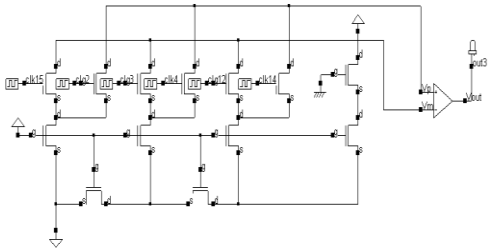

Fig B -3 bit R-2R ladder with operational amplifier

3.1 Open Loop Gain

The op-amp in this DAC is used in unity feedback configuration.

The closed loop gain for an op-amp is given by A/(A+1), where A is the open loop gain

The error Vout/Vin is highest at the highest possible V which is Vref=2V

3.2 Gain Bandwidth

For a maximum operating frequency of 25 MHz, the output needs to be settled in 40ns
Again as in the calculation of the open-loop gain, the maximum speed is needed when the output voltage is the highest i.e. 5V

4.9976=5(1-e^(-t/RC))

RC=5.2ns
Or the gain bandwidth comes out to be 20 MHz

3.3 first stage of Operational amplifier

The first stage of the op-amp as shown in the fig gives a gain of about 45-60 from a common mode range of 3-4V.

Sizes of the transistors are given in fig.

The lengths of transistors had to be increased to provide high small signal output impedance for a high gain.

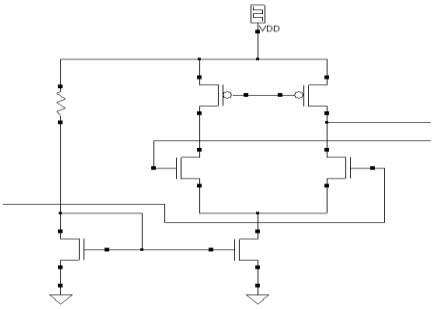

Fig C -1st stage of Op-Amp circuit

The second stage of the op-amp is acts as a gain stage and to provide enough current to drive a load of 20pF. The compensation capacitor was placed to improve the bandwidth of the amplifier.

Taking parasitic and load capacitance in to account, the maximum frequency of the second pole was calculated to be

1/RC = gm2/(C1+C2)

Where C1 and C2 are given from the figure as below

C1= Cgd1 +Cgd3 + Cdb1 + Cdb3 + Cgs5

C2= Cc+ Cdb5

Cl= Cc+Cgd5

gm2= gm5

c1+ c2 can be taken as 20pf as parasitic are negligible as compared to load capacitor Hence gm2 comes out to be 6.2 mA/V

And from the formula

gm = 2I/(Vgs -Vt)

I= bias current in second stage is calculated to be 2.3 mA

The 1st pole is arbitrarily chosen to lie at 16 KHz
And the 2nd pole is calculated to be 50 MHz

A resistor is placed in series with the capacitor so that the zero does not interfere in the transfer function of the gain.

The compensation capacitor is calculated to be 6.44 pF
And the zero resistors is calculated from the formula

Rz = (Cl+Cc)/gm5*Cc

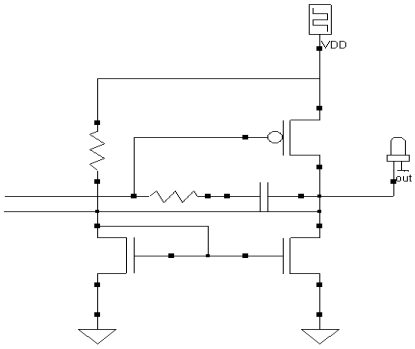

Fig D - 2nd stage of Op-Amp circuit

IV. PRE LAYOUT SIMULATION:

The characterization methods of the CMOS R-2R ladder D/A converter described in the previous section have been applied to a 3-bit D/A converter fabricated using the 0.13u CMOS process. The circuit diagram of the D/A converter is shown in Fig. A.

By applying input volts=2.0v as a pulse and digital input from 000 to 111 we achieved respective voltage and observe respective parameters like INL and DNL Offset, Glitch etc.

1. Integral Nonlinearity

INL = Output value for input code *n* - Output value of the reference line at that point.

Here input bits are from 000 to 111 which are represented here by 0 to 7. And Y axis shows ideal and actual INL. Maximum INL is O.43. Offset error must be corrected otherwise it will be replicated in all stage as INL errors.

Value of resister must be fixed so R and 2R will be generated. Main error is generated due to mismatch in the matching of resisters values. V_{DS} and I_D will be crucial parameter with W and L.

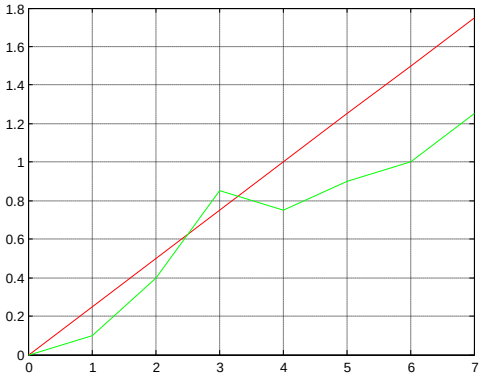

Fig E- Integration nonlinearity

2. Differential Nonlinearity

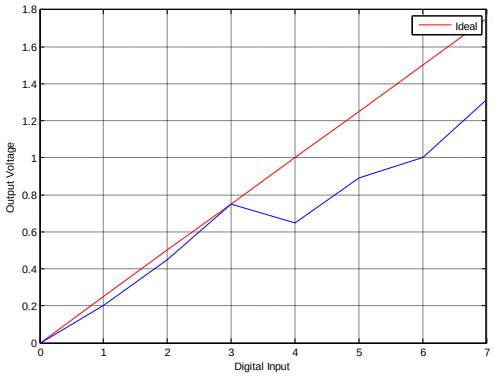

Fig F- Differential nonlinearity

Here input bits are from 000 to 111 which are represented here by 0 to 7. And Y axis shows ideal and actual DNL. Maximum DNL is O.36.

4. Glitch

Here At the starting of input we find glitch which is biggest error and provide less resolution. This problem can be corrected by proper matching of resister value and Width and length of the resister.

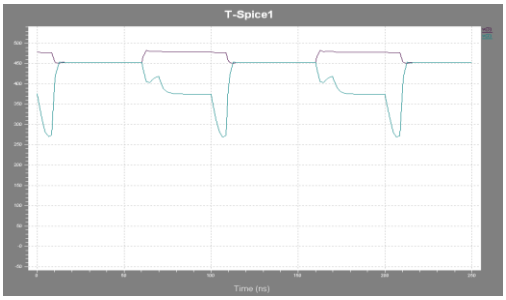

Fig G- Glitch at the output wave

5. Operational amplifier response

Here is the response of operational amplifier

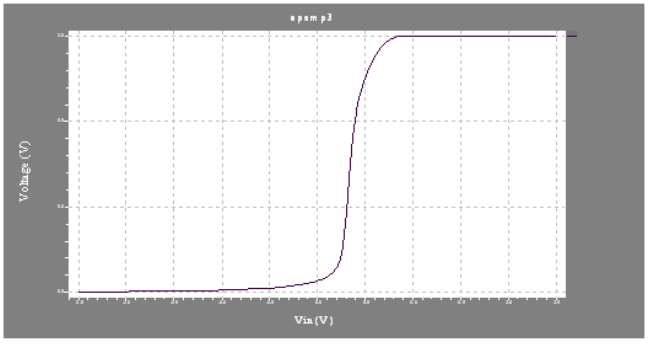

Fig I- Operational amplifier response

V. Results and Conclusion

High resolution and linearity is also achieved with this all characteristics given below, this can be improved by adding more stages of R-2R.

TABLE-I
Design Specification

Parameter	Design Specification & results
Technology	0.13um
Offset	32.0mV
INL	0.43
DNL	0.36
Glitch	Observed

The R-2R DAC is designed in TSMC 0.13um standard digital CMOS process and by using tanner tool.

DAC DNL/INL summary
DAC choice of architecture has a significant impact on DNL
INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
And better INL and DNL can be achieved by proper matching of resister s value in the CMOS circuit diagram.

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